INTERCONNECT SYSTEMS
a molex company

X6-250M

V1.7 07/31/2019

XMC Module with Eight 310 MSPS, 14-bit A/Ds, Xilinx Virtex-6 FPGA, and 4 GB LPDDR2

FEATURES

- Eight 310 MSPS, 14-bit A/D channels (250 MSPS built prior to Sep 10, 2014)
- Input Bandwidth: 400 MHz (AC-coupled)
- 1.32 Vp-p, AC-coupled, 50 ohm, SSMC inputs (1.5 Vp-p, AC-coupled, 50 ohm, SSMC inputs built prior to Sep 10, 2014)
- Xilinx Virtex-6 SX475T/SX315T/LX240T
- 4 banks of 1 GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCI Express providing 3.2 GB/s sustained transfer rates (-2 FPGA Required)
- Digital IO: 32-bits LVDS/64-bit LVCMOS
- XMC module (75x150 mm)
- 18 – 22 W typical
- Conduction cooling per VITA 20
- Ruggedization Levels for wide temperature and Vibration/Shock
- Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver
- WLAN, WCDMA, WiMAX Front-end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux/VxWorks Drivers
- C++ Host Tools

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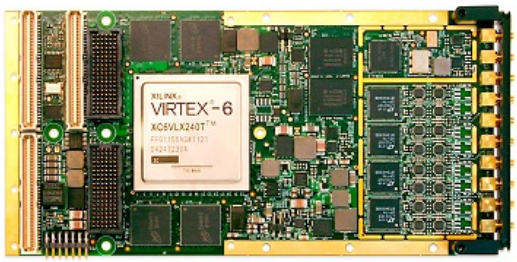

X6 250m

DESCRIPTION

The X6-250M integrates digitizing with signal processing on a PMC/XMC IO module. The module has a powerful Xilinx Virtex-6 FPGA signal processing core, and high performance PCI Express/PCI host interface. Applications include software-defined radio, RADAR receivers, and multi-channel data recorders.

The X6-250M has eight simultaneously sampling A/D channels that sample at rates up to 310 MSPS (14-bit). The A/D have matched input delays and response. The A/D are supported by a programmable sample clock PLL and triggering that support multi-card synchronization for large scale systems.

A Xilinx Virtex-6 SX315T (LX240T and SX475T options) with 4 banks of 1 GB DRAM provide a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The X6-250M has both XMC and PCI interfaces, supporting PCI Express or older PCI systems. The PCI Express interface provides up-to 3.2 GB/s sustained transfers rates through a x8 PCI Express Gen2 interface. System expansion is supported using secondary PCI Express or Aurora port used as a private data channel or second system bus.

The X6-250M power consumption is 18W for typical operation. The module may be conduction cooled using VITA 20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

The FPGA logic can be fully customized using VHDL and Matlab and the Frame Work Logic tool set. The Matlab BSP supports rapid development using the graphical block diagram Simulink environment with Xilinx System Generator. IP cores for many wireless and DSP functions, such as DDC, PSK/FSK demodulation, OFDM receiver, correlation, and low latency FFT, are available.

Software tools for host development include C++ libraries and drivers for Windows, Linux, and VxWorks. Application examples demonstrating the module features are provided.

X6-250M

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X6-250M	80279-<CFG>-<ER>	PMC/XMC module with eight 310 MSPS, 14-bit A/Ds, AC/DC coupled, Virtex-6 FPGA, 4 GB DRAM. <CFG> is configuration. **7**: LX240T2, DC-coupled, **8**: LX240T2, AC-coupled, **9**: SX315T2, AC-coupled, **10**: SX315T2, DC-coupled, **11**: SX475T2, AC-coupled, **12**: SX475T2, DC-coupled, **14:** SX315T2, DC-DC-DC-DC-AC-DC-AC-DC-coupled, **15:** SX315T2, AC-coupled, 310 MSPS, **16:** LX240T2, DC-coupled, custom config., **17:** SX475T2, DC-DC-DC-DC-AC-AC-AC-AC-coupled, **18:** SX475T2, AC-AC-DC-DC-AC-AC-DC-DC-coupled, **19:** SX475T2, AC-AC-DC-DC-AC-AC-DC-DC-coupled, with SSMB 10 Position Connector Housing (Delta Electronics P/N 2469000G91P-012) <ER> is environmental rating **L0...L4**.
Logic Development Package		
X6-250M FrameWork Logic	55039	X6-250M FrameWork Logic board support package for RTL and Matlab. Includes technical support for one year.
Cables		
SSMC to BNC cable	67150	IO cable with SSMC (male) to BNC (female), 1 meter
Adapters		
XMC-PCI Adapter	80167-0	PCI carrier card for XMC PCI Express modules, 64-bit PCI
XMC-PCIe Adapter	80259-0	PCI Express carrier card for XMC PCI Express modules, x8 lanes
XMC-Compact PCI/PXI Adapter	80207	3U compact PCI carrier card for XMC PCI Express modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
XMC-Cabled PCIe Adapter	90181-1	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
VPX Adapter	80262	3U VPX adapter for X6. Air-cooled or conduction-cooled versions. REDI covers available.
Embedded PC Host		
eInstrument-PC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Intel i7 CPU; Windows, Linux

eInstrument-PC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or i7 CPU; Windows, Linux
VPXI-ePC: 3U VPX PC with 4 expansion slots	90271	3U VPX embedded PC with 4 expansion slots, integrated timing and data plane; Intel i7 CPU; Windows, Linux
Heatsinks		
Standard Adapter (VPX, PXIe, DAQ-Node, eInstrument-PC, XMC-PCIe Adapter)	61548-1	Assembly, Heatsink Hardware, X6, XA on PXIe, VPX, ePC, DAQ-Node, XMC-PCIe Adapter
Standard Adapter (ePC-Duo)	Not Needed	EPC-Duo has the correct heatsinks installed.
Standard Adapter (SBC-Nano)	61543-1	Assembly, Heatsink Hardware, X6, XA on ePC-Nano

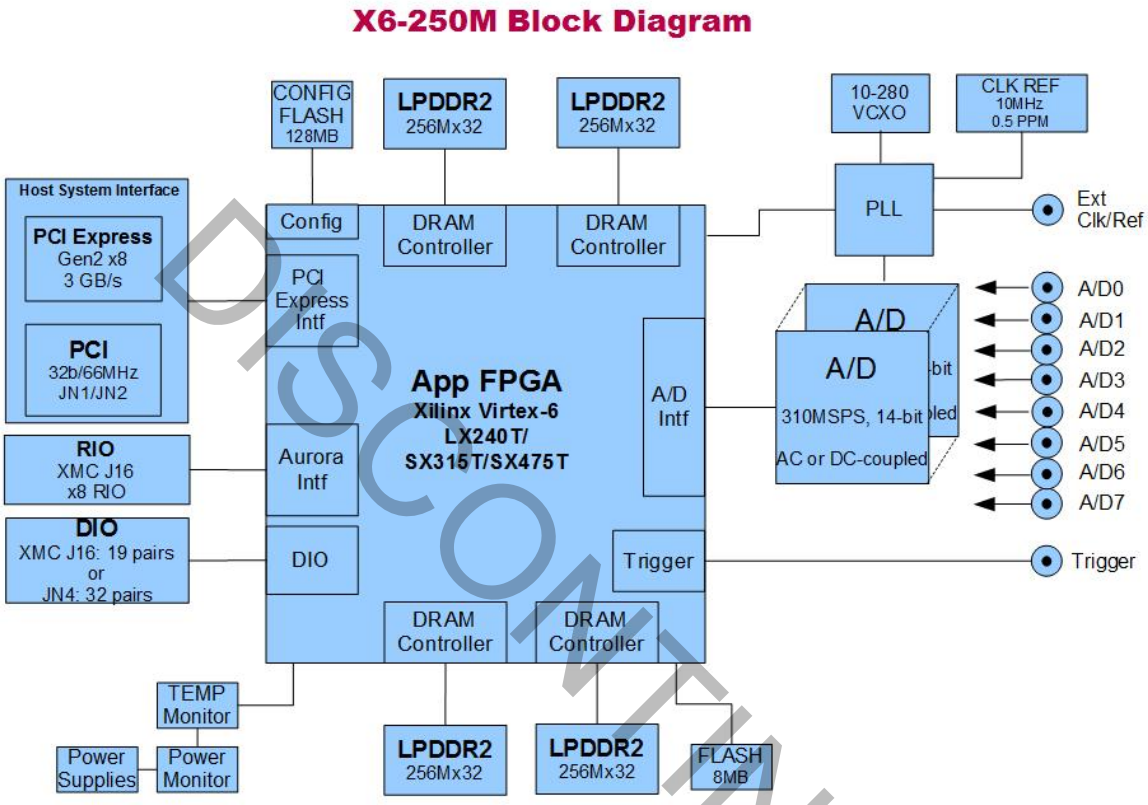

Figure 1. Block diagram

Operating Environment Ratings

X6 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. Click this link "Ruggedization Levels" to see the Ruggedization Levels available.

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

X6-250M

Standard Features

Analog	
Inputs	8
Input Range	1.32Vp-p 1.5 Vp-p (built prior to Sep 10, 2014)
Input Type	Single ended, AC or DC coupled
Input Impedance	50 ohm
A/D Device	Linear Tech LTC2157-14 (310 MSPS)
A/D Resolution	14-bit
A/D Sample Rate	10 MHz to 250 MHz
Input Bandwidth	400 MHz (-3dB) (AC-Coupled)

FPGA	
Device	Xilinx Virtex-6
Speed Grade	-1 or -2
Size	SX315T: ~31M gate equivalent
Flip-Flops	SX315T: 393K
Multipliers	SX315T: 1,344
Slice	SX315T: 49,200
Block RAMs	SX315T: 1,408 (25344 Kbits)
Rocket IO	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
DRAM Size	4 GB; 4 banks of 1 GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	Up to 5.2 GB/s sustained transfer rate per bank (333 MHz clock)

X6-250M

Host Interface	
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen 2 (x4 for -1 speed FPGA, x8 for -2 speed FPGA)
PCI Express Sustained Rate	3.2 GB/s (Gen2 x8) 1.2 GB/s (Gen2 x4 or Gen1 x8)

Clocks and Triggering	
Clock Sources	PLL or External
	0.3125 to 250 MHz
PLL Reference	External or 10 MHz on-board 10 MHz ref is +/-250 ppb -40 to 85 C
PLL Resolution	100 KHz Tuning Resolution
Phase Noise	-130 dBc @100 kHz
Triggering	External, software, acquire N frame
Ext Trigger Timing	Rise time < 1.0 uS
Ext Trigger Level	0.5 – 2.5 Vpp
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (J4/J16)	
Rocket IO Channels	8 (J16)
Rocket IO data rate	5 Gbps/lane (4 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	32 (J16/J4)
Signal Standard	LVCMOS (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC J4/XMC J16

Power	
Consumption	18W (VPWR = 5V, 1 DDR bank and no Aurora ports instantiated, 4 lane PCIe) 25W (VPWR = 12V, 4 DDR banks, all Aurora ports, 4 lane PCIe)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

X6-250M

ELECTRICAL CHARACTERISTICS At 24C ambient.			
Parameter	Typ	Units	Notes
A/D Performance – AC coupled			
Analog Input Bandwidth	400	MHz	-3dB
SFDR	77	dB	71 MHz sine input, 85%FS, Fs = 250 MSPS
S/N	65.1	dB	71 MHz sine input, 85%FS, Fs = 250 MSPS
THD	76.3	dB	71 MHz sine input, 85%FS, Fs = 250 MSPS
ENOB	10.5	bits	71 MHz sine input, 85%FS, Fs = 250 MSPS
Channel Crosstalk	-90 -60	dB dB	101 MHz sine input, 7dBm non-adjacent channel input, Fs = 250 MSPS 101 MHz sine input, 7dBm adjacent channel input, Fs = 250 MSPS (Typical) Non-adjacent channels is likely to be substantially better.
Noise Floor	-115	dB	Input grounded, Fs = 250 MSPS, 64K sample FFT, non-averaged
Gain Error	0.05	% of FS	Calibrated
Offset Error	< 1.0	mV	Calibrated
A/D Performance – DC Coupled			
Analog Input Bandwidth	550	MHz	-3dB
SFDR	70.7	dB	101 MHz sine input, 85%FS, Fs = 250 MSPS
S/N	59.9	dB	101 MHz sine input, 85%FS, Fs = 250 MSPS
THD	75.1	dB	101 MHz sine input, 85%FS, Fs = 250 MSPS
ENOB	9.6	bits	101 MHz sine input, 85%FS, Fs = 250 MSPS
Channel Crosstalk	-90 -60	DB dB	101 MHz sine input, 7dBm non-adjacent channel input, Fs = 250 MSPS 101 MHz sine input, 7dBm adjacent channel input, Fs = 250 MSPS (Typical) Non-adjacent channels is likely to be substantially better.
Noise Floor	-100	dB	Input grounded, Fs = 250 MSPS, 64K sample FFT, non-averaged
Gain Error	0.05	% of FS	Calibrated
Offset Error	< 1.0	mV	Calibrated

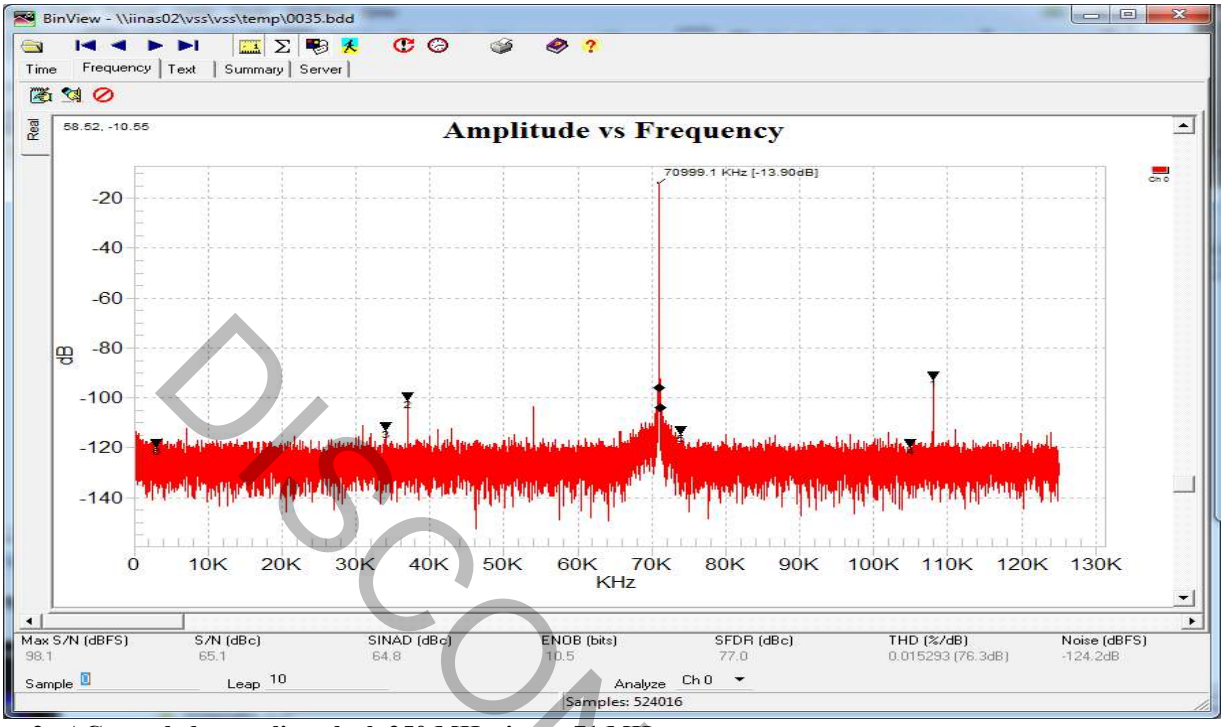

Figure 2. AC coupled, sampling clock 250 MHz, input 71 MHz

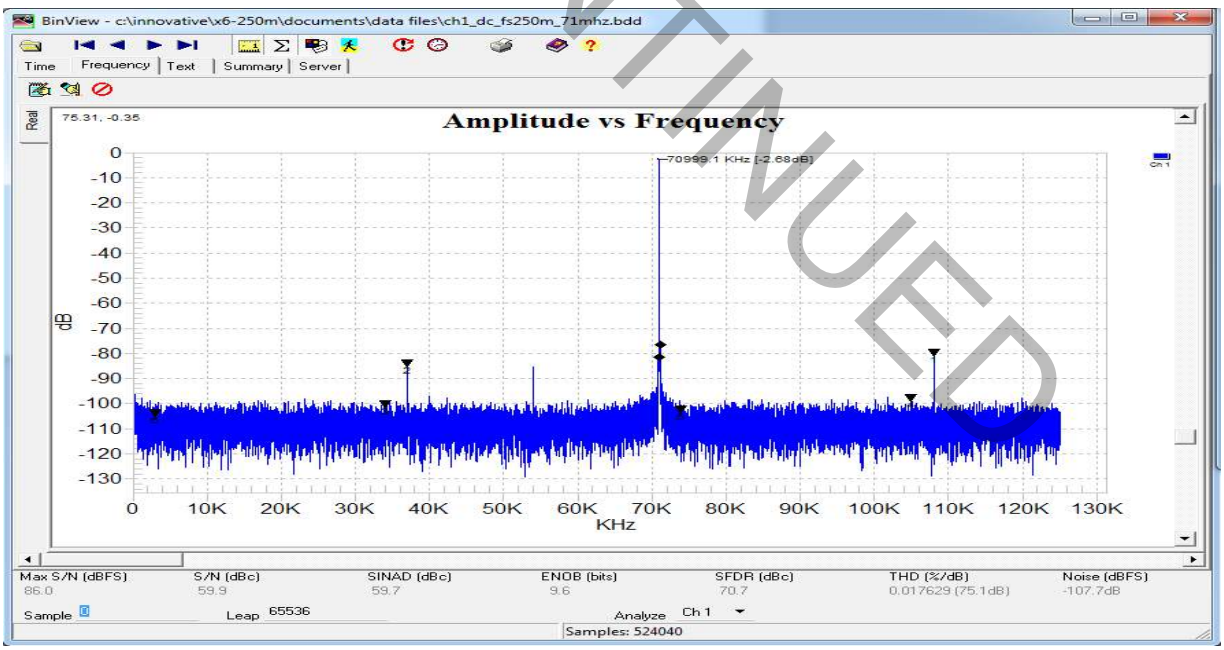

Figure 3. DC coupled, sampling clock 250 MHz, input 71 MHz

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Input Channel	Ch0 dB	Ch1 dB	Ch2 dB	Ch3 dB	Ch4 dB	Ch5 dB	Ch6 dB	Ch7 dB
0	-3.57	-61.63	-103	60.31	-97.73	-98.99	-97.73	-97.19
1	-61.7	-3.89	-101	-100	-96.08	-97.1	-96.5	-97.25
2	< -97	-89.35	-3.54	87	-96.43	-70.29	-97.91	-96.25
3	-72.86	-97.29	-61.69	-3.3	-97.14	-97.3	-97.18	-97.92
4	-97.2	-98.3	-97.4	-98	-2.94	-61.19	-97.06	-70.61
5	-98.39	-98.5	-69.89	-98.63	-61.52	-2.9	-97.27	-97.11
6	-97	-95	-98.4	-97.67	-96.23	-96.47	-3.64	-59.91
7	-96	-101	-97.3	-97.51	-69.53	-97.82	-60.25	-2.76

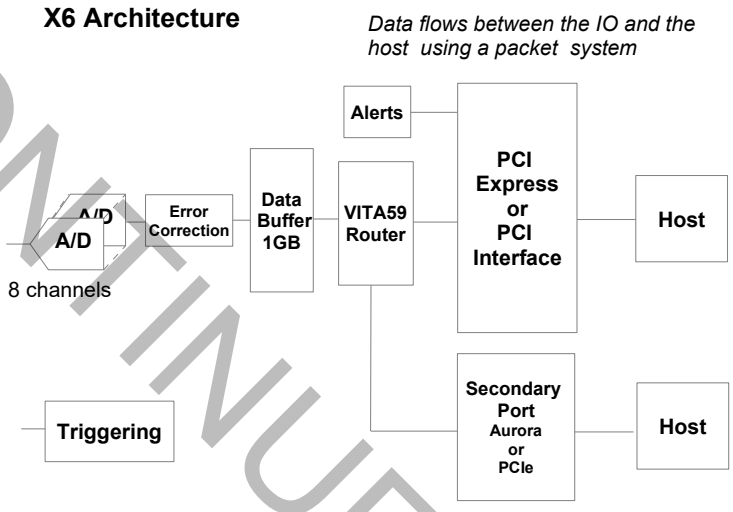
Figure 4. Crosstalk AC-Coupled

Input Channel	Ch0 dB	Ch1 dB	Ch2 dB	Ch3 dB	Ch4 dB	Ch5 dB	Ch6 dB	Ch7 dB
0	-3.57	<-90	<-90	60.31	<-90	<-90	<-90	<-90
1	<-90	-3.89	<-90	<-90	<-90	<-90	<-90	<-90
2	<-90	<-89	-3.54	<-90	<-90	-62	<-90	<-90
3	-60	<-90	<-90	-3.3	<-90	<-90	<-90	<-90
4	<-90	<-90	<-90	<-90	-2.94	<-90	<-90	-62
5	<-90	<-90	-63	<-90	<-90	-2.9	<-90	<-90
6	<-90	<-90	<-90	<-90	<-90	<-90	-3.64	<-90
7	<-90	<-90	<-90	<-90	-63	<-90	<-90	-2.76

Figure 5. Crosstalk DC-Coupled

Architecture and Features

The X6-250M module architecture integrates analog IO with an FPGA computing core, memories and PCI host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding applications in wireless, RADAR and medical imaging applications.



Analog IO

The X6-250M module has eight simultaneously sampling 14-bit, 310 MSPS A/D inputs. The analog input bandwidth is 400 MHz for wideband and direct sampling applications. The A/Ds are directly connected to the FPGA where the interface logic receives the data and performs digital error correction. A non-volatile ROM on the card is used to store the calibration coefficients and card information is programmed during factory test.

The A/D channels operate synchronously and sample simultaneously using either the PLL or external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple card systems can sample simultaneously when an external clock or reference is used by all cards.

FPGA Core

The X6 Module family has a Virtex-6 FPGA and memory at its core for DSP and control. The Virtex-6 FPGA is capable of over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. The FPGA fabric integrates logic, memory and connectivity features that enable high performance computing and sustained real-time performance.

The FPGA has direct access to four banks of 1 GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. Memory controller components include a buffer that uses the DRAM as a large FIFO for sample

buffering.

The X6 module family uses the Virtex-6 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. Logic utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 3.2 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCI Express controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex-6 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 40 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 400 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

PCI Host Interface

The X6 family can be optionally configured with a PCI interface capable of over 200 MB/s sustained rates. The Velocia architecture is the same as the PCI Express system, supporting the packet system with DMA.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard logic uses these lanes as two Aurora ports of 4 lanes each. Other protocols such as PCI Express, SRIO and SFPDP may be implemented in the FPGA.

J4 connector has 32 digital lines that connect to the FPGA. These digital IO lines are direct connections to the FPGA.

Module Management

The X6 family has independent temperature monitoring for the FPGA die. The temperature sensor is set so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the card easier to integrate into larger systems.

FPGA Configuration

The modules uses a FLASH memory for the Virtex-6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a “golden” image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and Matlab. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

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Software Tools

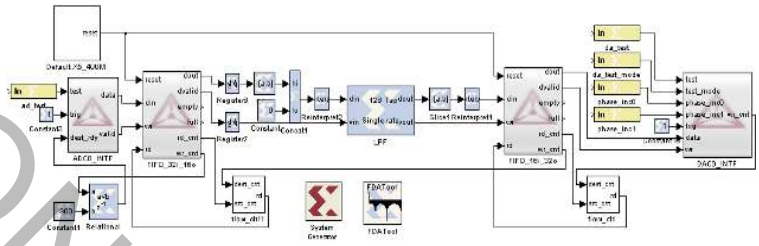
Software development tools for the module provides comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to Matlab for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The FrameWork Logic tools provide support for RTL and Matlab developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build up-on the Innovative components for packet handling, hardware interfaces, and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using Matlab Simulink for Logic Design

The Matlab Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into Matlab Simulink for rapid testing and development. This is an extremely powerful design methodology, since Matlab can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

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Digital Receiver

Digital Receiver is a turnkey solution providing integrated data logging, digital down-conversion (DDC), spectrum analyzer (FFT) in the compact system. The solution consists of three parts: the FPGA-based analog digitizer module, an eInstrument PC, and the firmware/software package to capture and analyze the data immediately.

A development kit is available to support creation of advanced custom firmware by logic developers. Netlist versions of the IP cores used to build the Digital Receiver are provided, so developers can integrate with their own custom cores to create an enhanced receiver design.

Product	DDC	FFT
V601	8 channels; bandwidth: 2 KHz – 50 MHz	1ch, 32K
V602	128 channels; maximum bandwidth: 420 KHz	No

Table 1. Digital receivers

Part Number	Target Module	Product	Description
55200-1	X6-250M	DDC and Spectrum Analysis	Framework Logic - 8 channels of IP-DDC and 1 channel of IP-FFT32K for Virtex-6 SX475T2
55200-2	X6-250M	Tunable DDC – 128 Channels	Framework Logic - Tunable 128 channels of IP-DDC128 for Virtex-6 SX475T2

Table 2. Development kits

Part Number	Target Module	Product	Description
55100-1	X6-250M	DDC and Spectrum Analysis	Package - 8 channels of IP-DDC and 1 channel of IP-FFT32K for Virtex-6 SX475T2
55100-2	X6-250M	Tunable DDC – 128 Channels	Package - Tunable 128 channels of IP-DDC128 for Virtex-6 SX475T2

Table 3. Software/firmware package

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Cables

The X6-250M module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SSMC male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCI Express or PCI system.

The X6 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with digital IO signals provide support for data transfer rates up to 3.0 GB/s sustained, as well as sideband signals for control and status. Protocols such as PCI Express and Aurora may be implemented for host communications or custom protocols.

Note that the high speed serial IO lanes require a host card electrically capable of supporting the high speed signal pairs such as 80259-0.

eInstrument DAQ-Node (90181-1) x1 PCIe to XMC 1U x 1/4 rack width 	**PCIe-XMC Adapter x8 lane (80259-0)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors DIO to MDR68 Preferred for X6 Modules 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 
VPX-XMC Adapter (80262-6) 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers 			

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X6 modules. The

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VPXI system supports multiple card systems with integrated timing and data plane features.

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC
Intel Core2Duo or low power Atom available
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
100 MB/s, 400 GB data logger
9-18 VDC operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent
Supports standalone operation for X6 modules

3U VPX PC with Four Expansion Slots and Integrated Timing (90271)

3U VPX, air-cooled chassis with backplane
Runs Windows, Linux, VxWorks
Intel Dual Core i5 or i7, 8GB, 256MB SSD
4x USB, GbE, x8 cable PCIe, Display port
Integrated timing clocks and triggers with GPS option
400 MB/s, 1TB data logger
AC or DC operation

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